In The Drawings:

Please substitute the attached clean drawing of Fig. 8 for the pending drawing of Fig. 8. The "Four times clock frequency signal of 266 MHz" in the pending Fig. 8 is amended to "Eight times clock frequency signal of 266 MHz" in the amended Fig. 8 because of typing error.

REMARKS

Present Status of the Application

The Office Action rejected all presently-pending claims 1-11. Specifically, the Office Action rejected claims 1, 2, 5 and 6 under 35 U.S.C. 102(b), as being anticipated by Pettey et al. (U.S. 6,067,590, hereafter Pettey). The Office Action also rejected claims 3 and 7 under 35 U.S.C. 103(a) as being unpatentable over Pettey, and further in view of US Patent Number 6,163,826 to Khan et al (hereafter Khan). The Office Action also rejected claims 4 and 8 under 35 U.S.C. 103(a) as being unpatentable over Pettey, and further in view of US Patent Number 6,507,879 to Sayles et al (hereafter Sayles). The Office Action rejected claims 9 and 10 under 35 U.S.C. 103(a), as being unpatentable over Pettey and Sayles. The Office Action rejected claim 11 under 35 U.S.C. 103(a), as being unpatentable over Pettey and Sayles, and further in view of Khan. After entry of the foregoing amendments, claims 1-11 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections-35 U.S.C. 102(b)

The Office Action rejected claims 1, 2, 5 and 6 under 35 U.S.C. 102(b), as being anticipated by Pettey. Applicants respectfully traverse the rejections for at least the reasons set forth below.

To anticipate a claim under 35 U.S.C. 102(b), the reference must teach each and every elements/features/steps of the claim. See M.P.E.P. § 2131.

With respect to claim 1, independent claim 1 recites the features as follows.

Claim 1. (Currently amended) A method of hot switching a data transfer rate on a bus, to dynamically switch the data transfer rate on the bus between a first control chip and a second control chip, comprising the steps of:

the first control chip and the second control chip receiving ***a transfer rate switching command***;

when either there is no data transaction processed or the data transaction process is finished, the first control chip issuing ***a bus release connect command***;

the first control chip and the second control chip entering into ***the bus release connect state*** according to the bus release connect command;

either the first control chip or the second control chip issuing ***a bus re-connect command***; and

the first control chip and the second control chip ***re-connecting*** to the rated-changed bus according to the transfer rate switching command. **(emphasis added)**

Independent claim 1 is allowable for at least the reason that Pettey does not disclose, teach, or suggest the features that are highlighted in claim 1 above.

Pettey teaches a method of transferring data on a data bus. The method includes driving a signal on a data bus by a first bus agent, sampling the signal at a second bus agent, storing the sampled signal in a storage medium associated with the second bus agent, and processing the stored signal at the second bus agent.

More specifically, in re Pettey, PCI bus 110 is between the host-to-PCI bridge 109 and the PCI-to-IAS bridge 130. The PCI bus 110 and PCI 2.1 bus agents is operable at maximum frequency of either 33 MHz or 66 MHz. PCI 2.1 buses and agents will operate a 66 MHz only if the bus and all bus agents are operable at 66 MHz. (See Pettey Column 9 Lines 40-47). Besides, using another bus and bus agent type, called registered mode, the maximum operating frequency of the registered bus may be limited to the maximum common operation frequency of the bus and all its attached bus agents. Furthermore, registered mode operation is implemented only if all bus agents are operating in registered mode. (See Pettey Column 9 Lines 61-67). If the bus and all devices on the bus are designed to use registered mode, then the PCI bus speed is set to 66 MHz registered mode, or the bus is operated at 66MHz or 33MHz. (See Pettey Column 11 Lines 1-6).

Therefore, the bus speed in Pettey is limited by the type of the bus and the bus agents. And, after system initialization, the bus speed in Pettey is fixed and cannot dynamically switched. In system operation, Pettey does not disclose the host-to-PCI bridge 109 and the PCI-to-ISA bridge 130 may enter into a "disconnect" state.

Pettey does not teach how to dynamically switch bus speed between low and high transfer rate without system rebooting. Pettey does not teach the north-bridge and the south-

bridge both receive a transfer rate switching command, and then the north-bridge issues a bus release connect command to make both north-bridge and the south-bridge enter a temporary "disconnect (bus release connect)" state. Pettey does not teach the north-bridge and the south-bridge both re-connect to the rate-changed bus after a bus re-connect command is issued.

Thus, Pettey does not anticipate claim 1, and the rejection should be withdrawn.

If independent claim 1 is allowable over the prior art of record, then its dependent claim 2 is allowable as a matter of law, because this dependent claim contains all features/elements/steps of independent claim 1. Additionally and notwithstanding the foregoing reasons for the allowability of claim 1, the dependent claim recites further features/steps and/or combinations of features/steps (as is apparent by examination of the claims themselves) that are patentably distinct from the prior art of record. The host-to-PCI bridge 109 in Pettey permits signals on the PCI bus 110 to be compatibly exchanged with signals on the processor host bus. (See Column 3, Lines 22-24) A north-bridge chip provides an interface between a system bus and a VLINK bus. Therefore, the host-to-PCI bridge 109 in Pettey is not a north-bridge chip. The PCI-to-ISA bridge 130 in Pettey provides a connection between PCI bus signals and an ISA bus. (See Column 3, Lines 30-32) A south-bridge chip provides an interface between a VLINK bus and a PCI bus. Therefore, the PCI-to-ISA bridge 130 in Pettey is not a south-bridge chip.

Regarding to claim 5, Claim 5 recites:

> 5. (Currently amended) A method of hot switching a data transfer rate on a bus, comprising the steps of:
>
> receiving a transfer rate switching signal before data transfer on the bus between a first control chip and a second control chip is interrupted; and
>
> when the first control chip and the second control chip are ***in a bus release state and then re-connecting***, providing ***another data transfer rate*** to the bus according to the transfer rate switching signal.***(emphasis added)***

Pettey does not teach a transfer rate switching signal is received before data transfer on a bus is interrupted. Pettey does not teach another data transfer rate is provided to the bus when the first control chip and the second control chip are re-connecting.

If independent claim 5 is allowable over the prior art of record, then its dependent claims 6 is allowable as a matter of law, because these dependent claims contain all features/elements/steps of their respective independent claim 1. Additionally and notwithstanding the foregoing reasons for the allowability of claim 5, the dependent claim recites further features/steps and/or combinations of features/steps (as is apparent by examination of the claims themselves) that are patentably distinct from the prior art of record.

Discussion of Office Action Rejections-35 U.S.C. 103(a)

The Office Action rejected claims 3 and 7 under 35 U.S.C. 103(a), as being unpatentable over Pettey, and further in view of Khan. The Office Action rejected claims 4 and 8 under 35 U.S.C. 103(a), as being unpatentable over Pettey, and further in view of Sayles. The Office Action rejected claims 9 and 10 under 35 U.S.C. 103(a), as being unpatentable over Pettey and Sayles. The Office Action rejected claim 11 under 35 U.S.C. 103(a), as being unpatentable over Pettey and Sayles, and further in view of Khan. Applicants respectfully traverse the rejections for at least the reasons set forth below.

In regarding claims 3 and 7, the Examiner correctly acknowledges that Pettey neither discloses nor suggests features in claim 1 and 5, and the data transfer rate switched between four times the north-bridge chip clock frequency and eight times the north-bridge chip clock frequency. Khan just discloses a clock speed programmable from 64KHz to 8 MHz. (See Khan, Column 4 Lines 34-36). However, Khan's bus interface (synchronous serial interface) is not a north-bridge chip. So, Khan does not teach the data transfer rate is switched between four times the north-bridge chip clock frequency and eight times the north-bridge chip clock frequency.

There would be no motivation for a skilled person to combine Pettey and Khan as proposed by the Examiner, as neither of the references explicitly suggests such a combination. In fact the only motivation for such a combination is provided by Applicants specification. For the reasons

below, Applicants disagree with the Examiner's argument that a skilled person would have combined Pettey and Khan to allow the data transfer rate switched between four times the north-bridge chip clock frequency and eight times the north-bridge chip clock frequency.

Applicant respectfully submits that both Pettey and Khan fail to disclose, teach, or even suggest at least all limitations emphasized above. Therefore, no combination of the teachings of the two references could possibly result in the invention as recited in claims 3 and 7.

Regarding claims 4 and 8, Sayles teaches command registers for setting the transfer rate of communication over the AGP bus, and if the AGP interface supports a high (2X) transfer rate but one of the graphics controllers supports only a low (1X) transfer rate, then the command registers are programmed to indicate the communication over the AGP bus is to proceed according to the 1X transfer rate. (See Sayles Column 5 Lines 23-33). So, the transfer rate over the AGP bus is determined by what graphic controller supports, and the transfer rate over the AGP bus is fixed and cannot be hot switched without system rebooting.

However, in this application, the transfer rate over the bus is based on the transfer rate switch command. The system is able to hot switch between a low bus transfer rate and a high bus transfer rate.

Applicant respectfully submits that both Pettey and Sayles fail to disclose, teach, or even suggest at least all limitations emphasized above. Therefore, no combination of the teachings of the two references could possibly result in the invention as recited in claims 4 and 8.

With respect to claim 9, independent claim 9 recites the features as follows.

Claim 9. (currently amended) A method of hot switching a data transfer rate on a bus, to dynamically switch a plurality of data transfer rates on the bus between a first control chip and a second control chip, comprising the steps of:

the first control chip and the second control chip receiving a ***data transfer rate switching command***, and temporarily storing the data transfer rate switching command into transfer rate registers of the first control chip and the second control chip;

when either there is no data transaction processed or the data transaction process is finished, issuing a ***bus release connect command*** to have the first control chip and the second control chip enter into a ***bus release connect state***; and

when either the first control chip or the second control chip issues a ***bus re-connect command***, the first control chip and the second control chip switching to one of the data transfer rates on the bus according to contents of the transfer rate registers. (emphasis added)

Applicant respectfully submits that both Pettey and Sayles fail to disclose, teach, or even suggest at least all limitations emphasized above. Therefore, no combination of the teachings of the two references could possibly result in the invention as recited in claim 9.

If independent claim 9 is allowable over the prior art of record, then its dependent claim 10 is allowable as a matter of law, because these dependent claims contain all features/elements/steps of their respective independent claim 9. Additionally and notwithstanding the foregoing reasons for the allowability of claim 9, the dependent claim 10 recites further features/steps and/or combinations of features/steps (as is apparent by examination of the claims themselves) that are patentably distinct from the prior art of record.

Regarding Claim 11, as above discussion, Pettey and Sayles do not teach limitations in Claim 10, and Khan's bus interface (synchronous serial interface) is not a north-bridge chip. So, Khan does not teach the data transfer rate is switched between four times the north-bridge chip clock frequency and eight times the north-bridge chip clock frequency.

Applicant respectfully submits that Pettey, Sayles and Khan fail to disclose, teach, or even suggest at least all limitations emphasized above. Therefore, no combination of the teachings of the references could possibly result in the invention as recited in claim 11.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-11 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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